Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-5 (cancelled)

6 (previously presented): An audio processing circuit for receiving a first stream complying with a first standard and generating a second stream complying with a second standard which is a digital interface standard, the first stream includes a plurality of frames, each of the frames includes a plurality of fields, the plurality of fields include a sync word field, the audio processing circuit comprises:

a stream buffer for storing the frames of the first stream;

a stream recovering circuit electrically connected to the stream buffer for receiving expected positions of the sync words derived from the first stream, determining if the expected positions of the sync words are correct, repeatedly increasing the expected positions by one position when the expected positions of the sync words are not correct, locating actual positions of the sync word fields, modifying the frames according to the actual positions of the sync word fields, and generating modified frames;

a first buffer electrically connected to the stream recovering circuit for storing the modified frames;

a burst circuit electrically connected to the first buffer for partitioning the modified frames into a plurality of payload sections, adding a preamble to each of the payload sections, and forming the second stream.

7 (original): The audio processing circuit of claim 6 wherein the second standard is S/PDIF standard.

8 (original): The audio processing circuit of claim 6 wherein the first stream is retrieved from an optical storage disk.

9 (original): The audio processing circuit of claim 6 further comprising:

a decoding circuit electrically connected to the stream buffer for decoding the frames retrieved from the stream buffer;

a second buffer electrically connected to the decoding circuit for storing decoded frames generated by the decoding circuit; and

a digital to analog converter electrically connected to the second buffer for converting the decoded frames received from the second buffer to analog signals.

10 (previously presented): The audio processing circuit of claim 9 wherein the decoding circuit and the stream recovering circuit are integrated into an audio processor of the audio processing circuit.

11-20 (cancelled)